CLAIMS

I Claim:

1. A method of operating a one-transistor, floating-body (1T/FB) dynamic random access memory (DRAM) cell having an underlying buried region, the method comprising:

biasing the buried region; and

writing a data bit to the 1T/FB DRAM cell using a hot carrier injection mechanism.

2. A method of operating a one-transistor, floating-body (1T/FB) dynamic random access memory (DRAM) cell having an underlying buried region, the method comprising:

biasing the buried region; and

writing a data bit to the 1T/FB DRAM cell using a junction forward bias mechanism.

3. A method of fabricating a one-transistor, floating-body (1T/FB) dynamic random access memory (DRAM) cell, method comprising:

forming a buried region having a first conductivity type below an upper surface of a semiconductor region of a semiconductor substrate, the semiconductor region having a second conductivity type, opposite the first conductivity type; and

forming a field-effect transistor in the semiconductor region over the buried region, wherein a depletion region is located between the buried region and source, drain and body regions of the field-effect transistor.

4. The method of Claim 3, wherein the buried region is formed by an ion implantation step.

5. The method of Claim 4, wherein the buried region is implanted through a first mask.

6. The method of Claim 5, further comprising performing a threshold voltage adjustment implant having the second conductivity type through the first mask.

7. The method of Claim 3, further comprising forming one or more shallow trench isolation regions that extend a first depth into the semiconductor substrate.

8. The method of Claim 7, further comprising implanting the buried region such that the buried region has a top interface located at or above the first depth in the semiconductor substrate, and a bottom interface located below the first depth in the semiconductor substrate.

9. The method of Claim 3, wherein the field-effect transistor is fabricated using a process compatible with a standard CMOS process.

10. The method of Claim 3, further comprising forming a well region having the first conductivity type in the semiconductor substrate, wherein the buried region contacts the well region.

11. The method of Claim 3, further comprising forming a deep well region having the first conductivity type in the semiconductor substrate, wherein the deep well region is located below and continuous with the buried region.

12. The method of Claim 11, further comprising forming a well region having the first conductivity type in the semiconductor substrate, wherein the well region contacts the deep well region.